TRANSMITTAL OF FORMAL DRAWINGS

Docket No.
00750452AA

In Re Application Of: **Park et al.**

Serial No.	Filing Date	Confirmation No.	Examiner	Art Unit
09/924,318	08/08/2001	3592	B. Tran	1765

Invention: **METHOD OF BUILDING A CMOS STRUCTURE ON THIN SOI WITH SOURCE/DRAIN ELECTRODES FORMED BY IN SITU DOPED SELECTIVE AMORPHOUS SILICON**

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Transmitted herewith are:

4 sheets of formal drawing(s) for this application.

☒ Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c).

This submission of formal drawings is in response to the Notice of Allowability mailed on January 5, 2004.

Marshall M. Curtis

Signature

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Dated: **January 8, 2004**

I certify that this document and attached formal drawings are being deposited on with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature of Person Mailing Correspondence

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